WHAT IS CLAIMED IS:

1. An apparatus comprising:

two or more accelerators, each of the accelerators comprising circuitry configured to perform a task for an application program; and

one or more resources coupled to the accelerators, the resources shared by the accelerators and configured to interface the accelerators to an interconnect and further configured to provide a programming interface for communication with the accelerators.

2. The apparatus as recited in claim 1 wherein the programming interface is used by the application program to communicate with the accelerators.

3. The apparatus as recited in claim 1 wherein the resources include an interface circuit configured to communicate on the interconnect.

4. The apparatus as recited in claim 3 wherein the resources include a control circuit configured to provide the programming interface.

5. The apparatus as recited in claim 4 wherein the programming interface comprises one or more memory-mapped commands, and wherein the control circuit is configured to decode the addresses of transactions on the interconnect to detect the commands and is further configured to transmit indications of the commands to a corresponding one of the accelerators.

6. The apparatus as recited in claim 4 wherein the control circuit includes one or more registers, and wherein the control circuit is configured to supply control signals to the

accelerators responsive to values in the registers.

7. The apparatus as recited in claim 4 wherein the control circuit includes one or more interrupt registers, and wherein the control circuit is coupled to receive interrupt information from any of the accelerators for storage in the interrupt registers for reading by a central processing unit (CPU) in response to an interrupt from the apparatus.

8. The apparatus as recited in claim 3 wherein the resources further comprise a first memory coupled to the interface circuit, the first memory including one or more entries for storing data accessed by the accelerators.

9. The apparatus as recited in claim 8 wherein the first memory is an input memory for storing data read by the accelerators, the input memory coupled to receive data from the interface circuit and to provide data to the accelerators.

10. The apparatus as recited in claim 8 wherein the first memory is an output memory for storing data written by the accelerators, the output memory coupled to receive data from the accelerators and to provide data to the interface circuit.

11. The apparatus as recited in claim 8 further comprising circuitry configured to provide access to the first memory by each of the accelerators.

12. The apparatus as recited in claim 3 wherein the resources further include a memory management unit (MMU) configured to translate virtual addresses provided by the application program to physical addresses for accessing a memory.

13. The apparatus as recited in claim 1 wherein the accelerators include one or more code translators.

14. The apparatus as recited in claim 1 wherein the accelerators include one or more decompressors.

15. The apparatus as recited in claim 1 wherein the accelerators include one or more parsers.

16. A carrier medium configured to hold a data structure representative of:

two or more accelerators, each of the accelerators comprising circuitry configured to perform a task for an application program; and

one or more resources coupled to the accelerators, the resources shared by the accelerators and configured to interface the accelerators to an interconnect and further configured to provide a programming interface for communication with the accelerators.

17. The carrier medium as recited in claim 16 wherein the programming interface is used by the application program to communicate with the accelerators.

18. The carrier medium as recited in claim 16 wherein the resources include an interface circuit configured to communicate on the interconnect.

19. The carrier medium as recited in claim 18 wherein the resources include a control circuit configured to provide the programming interface.

20. The carrier medium as recited in claim 19 wherein the programming interface comprises one or more memory-mapped commands, and wherein the control circuit is configured to decode the addresses of transactions on the interconnect to detect the commands and is further configured to transmit indications of the commands to a

corresponding one of the accelerators.

21. The carrier medium as recited in claim 19 wherein the control circuit includes one or more registers, and wherein the control circuit is configured to supply control signals to the accelerators responsive to values in the registers.

22. The carrier medium as recited in claim 19 wherein the control circuit includes one or more interrupt registers, and wherein the control circuit is coupled to receive interrupt information from any of the accelerators for storage in the interrupt registers for reading by a central processing unit (CPU) in response to an interrupt.

23. The carrier medium as recited in claim 18 wherein the resources further comprise a first memory coupled to the interface circuit, the first memory including one or more entries for storing data accessed by the accelerators.

24. The carrier medium as recited in claim 23 wherein the first memory is an input memory for storing data read by the accelerators, the input memory coupled to receive data from the interface circuit and to provide data to the accelerators.

25. The carrier medium as recited in claim 23 wherein the first memory is an output memory for storing data written by the accelerators, the output memory coupled to receive data from the accelerators and to provide data to the interface circuit.

26. The carrier medium as recited in claim 23 further comprising circuitry configured to provide access to the first memory by each of the accelerators.

27. The carrier medium as recited in claim 18 wherein the resources further include a memory management unit (MMU) configured to translate virtual addresses provided by the application program to physical addresses for accessing a memory.

28. The carrier medium as recited in claim 16 wherein the accelerators include one or more code translators.

29. The carrier medium as recited in claim 16 wherein the accelerators include one or more decompressors.

30. The carrier medium as recited in claim 16 wherein the accelerators include one or more parsers.

31. A method comprising:

selecting an interface circuit from a library of interface circuits dependent on a system into which an accelerator engine comprising the interface circuit is to be included;

selecting one or more accelerators from a library of accelerators dependent on which application tasks are to be accelerated; and

forming a data structure representing the accelerator engine by coupling a representation of the bus interface circuit, a representation of one or more shared resources, and a representation of the accelerators.

32. The method as recited in claim 31 wherein the data structure comprises a register transfer level description.

33. The method as recited in claim 31 wherein the one or more resources are described by one or more attributes, the method further comprising selecting values for the one or more attributes.

34. The method as recited in claim 33 wherein the resources including a first memory comprising one or more entries configured to store data accessed by the accelerators, wherein the attributes include a number of the one or more entries.

35. The method as recited in claim 31 wherein the one or more shared resources include one or more optional resources selectively included in the data structure.